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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,473	10/31/2003	Jonghee Han	2003P52883US	2763
46798	7590	08/28/2006		
PATTERSON & SHERIDAN, LLP Gero McClellan / Infineon Technologies 3040 POST OAK BLVD., SUITE 1500 HOUSTON, TX 77056			EXAMINER HASSAN, AURANGZEB	
			ART UNIT 2182	PAPER NUMBER

DATE MAILED: 08/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/699,473		HAN, JONGHEE	
	<b>Examiner</b>		<b>Art Unit</b>	
	Aurangzeb Hassan		2182	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 17 April 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-42 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                                   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>5/4/05</u>  | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Park (US Patent Number 6,147,926).

3. As per claims 1, 10, 23, 26, 27, 29, 39 Park teaches a method and device comprising,

In order to better assist the applicant to understand the Park reference the examiner makes note of the correlation of Park with the related art (figure 1). As described by Park in column 2, lines 36 – 47 Park's invention modifies related art in order to support a mode that is synchronized to both side edges of the system clock and the corresponding frequency. Therefore Park includes the teachings of the related art as it is a modification of it. Additionally in Park figure 1 elements 101, 102, 110, 240, 242 map to the applicant's figure 1 elements 101, 104, 110, 108, 107 respectively.

a bidirectional data bus (element 105, figure 1);

a first driver circuit coupled to the bus (FRDB, column 4, lines 40 – 42) and configured to propagate a first data and a second data in a first direction along the bus;

a first receiver circuit coupled to an end of the bus opposite the first driver circuit and configured to latch (FRDB latch, element 41, figure 2, column 4 line 39) the first and second data in response to a first strobe clock signal (FRDB strobe signal, column 4, lines 40 – 42);

a second driver circuit coupled to the bus (SRDB, column 4, lines 43 – 44) and configured to propagate a third data and a fourth data in a second direction along the bus;

a second receiver circuit coupled to an end of the bus opposite the second driver circuit and configured to latch (SRDB latch, element 42, figure 2, column 4, line 47) the third and fourth data in response to a second strobe clock signal (along the bidirectional bus between the I/O interface 110 and connecting circuit, figure 1);

a first controller configured to enable the first driver circuit and to generate the first strobe clock signal (first Enable, column 7 lines 1 – 16);

a second controller configured to enable the second driver circuit and to generate the second strobe clock signal (second Enable, column 7 lines 1 – 16);

a first strobe clock signal line (FRDB strobe signal, column 4, lines 40 – 42) to propagate the first strobe clock signal from the first controller to the first receiver circuit;

a first round-trip path comprising a first return path for the first strobe clock signal back to the first controller (column 6, 42 – 60, controller round-trip path, along the bidirectional bus between the I/O interface 110 and connecting circuit, figure 1);

a second strobe clock signal line (SRDB strobe signal, column 4, lines 43 – 45) to propagate the second strobe clock signal from the second controller to the second receiver circuit; and

a second round-trip path comprising a second return path for the second strobe clock signal back to the second controller (column 6, 42 – 60, controller round-trip path); and

(Claim 1) transmitting, via a first signal path, a strobe signal to a receiving circuit indicating the validity of the first data on the data bus (database controlling unit transmits SDO valid signal indicating validity of data, column 4, lines 35 – 56);

(Claim 10) receiving, by the controller, the strobe signal a period of time (latency controlling unit 36, figure 2, column 7, lines 1 – 22) after issuing the strobe signal;

(Claim 18) issuing a strobe signal to a receiving circuit via a forward signal path to indicate the presence of the first data on the data bus (database controlling unit transmits SDO valid signal indicating validity of data, column 4, lines 35 – 56); and

(Claim 29) a return clock signal line coupled at an output end to the controller and configured to propagate a return clock signal signaling the controller to enable the driver to drive the second data (QCLK sync unit 53, figure 2, column 5, lines 19 – 44); wherein the return clock signal is timed off of the strobe clock signal (DCLK, figure 2).

4. As per claim 2, Park teaches a method wherein driving the first data and the second data on the data bus comprises enabling a driver to drive the data (output driver, element 44, figure 2, column 4, lines 55 – 65).

5. As per claims 3 and 22, Park teaches a method wherein the data bus is an internal data bus of the multiple data rate memory device (column 4, lines 1 – 20).

The data bus taught by Park is internal to the DDR SDRAM thus internal to the memory device.

6. As per claims 4, 15, 24, 31, Park teaches a method wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory (DDR SDRAM) (DDR SDRAM, column 4, lines 14 – 16).

7. As per claims 5, 19, 30, Park teaches a method wherein a duration of time between issuing the strobe signal and receiving the return signal is at least as long as a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit (element 33, figure 2, column 4, lines 63 – 65).

8. As per claims 6 and 20, Park teaches a method wherein; a duration of time between issuing the strobe signal and receiving the return signal is substantially equal to a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit (element 33, figure 2, column 5, lines 1 – 7).

9. As per claim 7, Park teaches a method wherein the return signal is the strobe signal (column 4, lines 40 – 48, strobe signals).
10. As per claim 8, Park teaches a method further comprising generating the return signal by the receiving circuit (column 6, lines 27- 29 & 45 – 53).
11. As per claim 9, Park teaches a method wherein generating the return signal comprises buffering the strobe signal (output buffer, element 44, figure 2, column 5, lines 12 – 17).
12. As per claim 11, Park teaches a method wherein (a)-(f) are performed bidirectionally over the data bus (element 105, figure 1).
13. As per claims 12, 17, 25, Park teaches a method wherein the strobe signal is propagated to the receiving circuit on a first path and propagated to the controller on a second path, and wherein only a portion of each path shares a common line (database controlling unit, element 34, figure 2, column 6, lines 38 – 61).

Database controlling unit taught by Park, tied into the FIFO unit element 35 of figure 2 and the latency pipeline controlling unit element 36 of figure 2 allow for sharing a common line in a portion.

14. As per claim 13, Park teaches a method wherein the strobe signal is propagated to the receiving circuit on a first path and propagated to the controller on a second path, and wherein lengths of the first and second paths are substantially the same (column 6, lines 50 – 67).

15. As per claim 14, Park teaches a method comprising, latching the second data in from the data bus (SRDB latch, element 42, figure 2, column 4, line 47).

16. As per claim 16, Park teaches a method comprising:

(1) by a driver controller (element 34, figure 2): driving first data on a data bus (FRDB, column 4, lines 40 – 42); transmitting a data strobe signal to a receiver via a forward signal path (FRDB strobe signal, column 4, lines 40 – 42); receiving the data strobe signal via a return signal path; and in response to receiving the strobe signal, driving second data on the data bus (SRDB, column 4, lines 43 – 44); and (2) by a receiver (data path composition 32, figure 2): receiving the strobe signal via the forward signal path (FRDB strobe signal, column 4, lines 40 – 42); and in response to receiving the strobe signal, latching the first data in from the data bus (FRDB latch, element 41, figure 2, column 4 line 39).

17. As per claim 21, Park teaches a method wherein receiving the strobe signal by the control circuit occurs substantially simultaneously with receipt of the strobe signal by

the receiving circuit (database controlling unit, element 34, figure 2, column 6, lines 39 – 53).

18. As per claim 28, Park teaches a device wherein the round-trip path is partially defined by the strobe clock signal line (column 6, 42 – 60, controller round- trip path).

19. As per claim 32, Park teaches a circuit comprising:

a controller comprising a strobe clock signal output (strobe signal, column 4, lines 40 – 45) and a return clock signal input and configured to issue a first enable signal (first Enable, column 7 lines 1 – 16) and a second enable signal (second Enable, column 7 lines 1 – 16), the first enable signal enabling a plurality of drivers to drive respective first data on respective data lines, and the second enable signal enabling the plurality of drivers to drive respective second data on their respective data lines;

a strobe clock signal line coupled to the strobe clock signal output (SDO, column 4, lines 45 – 50); and

a return clock signal line coupled to the return clock signal input; wherein the strobe clock signal line defines an initial portion of a round-trip path and the return clock signal line defines a terminal portion of the round-trip path; and wherein the controller is configured to (column 5, lines 20 – 26);

respond to an external clock signal by pulling a strobe clock signal to a first state on the strobe clock signal line and pulling the first enable signal to an active state (column 7, lines 1 – 10);

receive a return clock signal on the return clock signal line a period of time after pulling the strobe clock signal to the first state, wherein the return clock signal is timed off of the strobe clock signal and indicates an assumed receipt of the strobe clock signal in the active state by receiving circuitry coupled to the respective data lines and configured to latch in the first (FRDB latch, element 41, figure 2, column 4 line 39) and second (SRDB latch, element 42, figure 2, column 4, line 47) data from the data lines in response to the strobe clock signal; and respond to the received return clock signal by pulling the second enable signal to an active state (column 7, line 4).

20. As per claim 33, Park teaches a circuit wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory (DDR SDRAM, column 4, lines 14 – 16).

21. As per claim 34, Park teaches a circuit wherein the strobe clock signal is coupled to the return clock signal line and to the receiving circuitry (elements 41 and 42, figure 2, coupled to FSRDB for receiving).

22. As per claim 35, Park teaches a circuit wherein the receiving circuitry is configured to latch (FRDB latch, element 41, figure 2, column 4 line 39) in the first data from the data lines in response to receiving the strobe clock signal in the first state and to latch (SRDB latch, element 42, figure 2, column 4, line 47) in the second data from

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the data lines in response to receiving a transition of the strobe clock signal from the first state to a second state.

23. As per claim 36, Park teaches a circuit wherein the return clock signal is a delayed instance of the strobe clock signal (element 33, figure 2, column 4, lines 60 – 65).

24. As per claim 37, Park teaches a circuit wherein the strobe clock signal and the return clock signal are issued within a single period of an external clock signal (element 33, figure 2, column 5, lines 19 - 29).

25. As per claim 38, Park teaches a circuit wherein the return clock signal is a delayed instance of the strobe clock signal (element 33, figure 2, column 4, lines 55 – 65).

26. As per claim 40, Park teaches a device wherein the first round-trip path is partially defined by the first strobe clock signal line (FRDB strobe signal, column 4, lines 40 – 42) and the second round-trip path is partially defined by the second strobe clock signal line (SRDB strobe signal, column 4, lines 43 – 45).

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27. As per claim 42, Park teaches a device wherein the first strobe clock signal line comprises at least a portion of the second strobe clock signal line (database controlling unit, element 34, figure 2, lines 35 – 50).

### ***Response to Arguments***

28. Applicant's arguments filed 4/17/06 have been fully considered but they are not persuasive. The applicant argue:

1) Park fails to disclose transmitting a strobe signal indicating validity of the first data on the data bus (page 12).

2.) Park fails to disclose receiving, by the controller, the strobe signal a period time after issuing the strobe signal (page 13).

3.) Parks fails to disclose a driver controller (page 14).

4.) Park fails to disclose issuing a strobe signal indicating presence of data (page 15).

5.) Park fails to disclose a return path for the strobing clock signal back to the controller (page 16).

6.) Park fails to disclose a return clock signal line timed off of the strobe clock signal enabling the driver to drive the second data (page 17).

7.) Park fails to disclose a return clock signal line coupled to the return clock signal input (page 18).

8.) Park fails to disclose a second driver propagating data in a second direction along the bus (page 19).

29. As per arguments 1 and 4, the Examiner disagrees. Park teaches a valid signal indicating presence and validity data on a bus (SDO valid signal, figure 2). Receiving the valid signal in assuring its validity it provides a driving signal for a data pulse (column 7, lines 54 – 62). Clearly from this citation, one of ordinary skill in the art would recognize that only after ensuring presence and validity would driving a data pulse be provided such that a start code is operable to detect a beginning position of reproduction data through an extraction circuit.

30. As per argument 2, the Examiner disagrees. Park teaches first and second Enable signals from the latency pipeline controlling unit 36, figure 2. Because latency is inherent in Park, in which the receiving a signal will always occur a period of time after it has been sent, the latency unit is what manages and provides synchronization with the clock and the controlling feature for the database-controlling unit (column 7, lines 2 – 22). Clearly from this citation, one of ordinary skill in the art would recognize that for a signal to be received it is inherent that it occurs a period of time after it has been sent.

31. As per argument 3, the Examiner disagrees. Park teaches a modification of the related art shown in figure 1, consisting of enhanced clock and frequency handling techniques. As figure 2 is an improvement of figure 1, the bidirectional attributes of the

buses, between the I/O interface and the input and output data paths, allow for Park's driving controller to transmit and receive the data strobe signals and inherently control driving of data via response on the data bus (column 6, lines 38 – 67). Clearly from this citation, one of ordinary skill in the art would recognize that the driving controller internalizes the strobe signal control and enables driving first and second data on data bus.

32. As per arguments 5 and 7, the Examiner disagrees. Park teaches a QCLK sync unit 53 in figure 4 that manages a strobing return clock signal back to the controller. The bidirectional bus interface figure 1 from element 102 reinforces the two-direction/return path configuration that Park's modification utilizes in enhancement. The clock.sync unit is internal to the latency unit that directly corresponds to the database-controlling unit (column 5, lines 19 – 34). Clearly from this citation, one of ordinary skill in the art would recognize that the controller has a return path on which a return strobe clock signal is present.

33. As per argument 6, the Examiner disagrees. Park teaches a clock which is timed off of the strobe clock, DCLK, which enables the operational driver. The clock QCLK is also coupled to the output driver/output buffer in figure 2 (column 4, lines 66 – 67, column 5 lines 1 – 18), all the clock signals are essentially timed off one another (column 5, lines 19 – 50). Clearly from this citation, one of ordinary skill in the art would recognize the driving functionality on the output end of the clock-generating unit.

34. As per argument 8, the Examiner disagrees. Park teaches data along the bidirectional bus between the I/O interface 110 and connecting circuit, figure 1 for the second driver propagating data. As Park is a modification of the related art it includes functionality that is inherent to invention. The related art as shown in figure 1 allows for a return path in a second direction for data to be driven (column 1, lines 58 – 67, column 2, lines 1 – 23). Clearly from this citation, one of ordinary skill in the art would recognize the bidirectional qualities of driving data in not only a first but also a second direction inherent in Park.

The examiner has provided additional citations to allow the applicant to better understand the rejections aforementioned.

### ***Conclusion***

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571) 272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

  
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SUPERVISORY PATENT EXAMINER  
7/28/06